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THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
KITOV, ZEEV V	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,059	LAI, HAN-CHUNG	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on April 12, 2006. Claims 1, 3, 5, 7 and 10 are amended. An Office Action follows.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1, 3, 5, 7, 10 are under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is in the claim limitations reciting " impedance of the ESD protection devices", while the Specification continuously recites "equivalent impedances". A meaning of the term is not clear. It is particularly not clear how this impedance is measured, and what components of the ESD protection circuit affect this parameter. It is not clear for example whether a connection trace resistance is a part of this impedance. The Specification is silent with regard to the term. This discrepancy makes the claims indefinite. Appropriate correction either in the claims or in the Specification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Saito et al. (US 2004/0026741 A1). Regarding Claims 1, AAPA discloses following elements: a mechanism for preventing ESD damage to a electronic device including at least one connection area having a plurality of pads (P1 to P n in Fig. 1) arranged sequentially for mounting to an integrated circuit, and a plurality of fan-out signal lines (F1 to Fn in Fig. 1) extending from the pads (P1 to P n in Fig. 1) respectively, the pads (P1 and P n in Fig. 1) disposed on outermost sides of the connection area, the mechanism including: a plurality of ESD protection device (ES1 to ES n in Fig. 1 and 2) configured corresponding to the fan-out signal lines (F1 to Fn in Fig. 1). It further discloses: "When ESD occurs in the TFT LCD panel, the ESD protection device of each signal line disposed on outermost sides of the connection area 10 has the longest path" (page 2, lines 11 – 17). Eventually, it affects the ESD dispersion and signal lines disposed on outermost sides of the connection area become the most vulnerable to the ESD. However, it does not disclose the ESD devices disposed on outermost sides of the connection area having smaller impedance than the other ESD protection devices. Saito et al. disclose the ESD protection devices (NT1 – NTn in Fig. 3) having unequal impedances, since each device in area B has it impedance composed of impedance of transistor (NTn through Ntm+1 in Fig. 3) and of additional silicide block (r + rAB in Fig. 3), while each device in area A has it impedance

composed of impedance of transistor (NT1 through NTm in Fig. 3) and of additional silicide block (r in Fig. 3). It further discloses compensation of impedances of the traces (AREA A and AREA B in Fig. 3) by varying the resistance of the ESD device (shown in Fig. 8, paragraph [0037]). An added correction is roughly proportional to the additional impedance of the connecting line. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the AAPA solution by setting the impedances of the ESD protection devices disposed on outermost sides of the connection area, i.e. ES1 and ES n, smaller than impedances of the other ESD protection devices, because (I) AAPA states that these lines are the longest and therefore have the highest impedance, which according to Saito et al., is to be compensated, and (II) as Saito et al. state (page 1, [0009] – [0011]), such correction will result in uniform distribution of the ESD load to the protective elements.

Regarding Claim 5, Saito discloses compensation of the trace impedance by varying the resistance of the ESD device silicide block. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the AAPA solution by setting the impedance of the ESD device such that an impedance of one ESD device ESk being different from impedances of other ESD devices (1<k< n), because the trace impedance depends on its length and for some signal lines, which according to AAPA, disposed on outermost side of the connection area 10 have the longest path, and their trace resistance is substantial, and therefore for compensation of

their resistances, the resistance of the silicide blocks of the particular ESD devices should be adjusted accordingly.

Regarding Claim 10, AAPA discloses a liquid crystal display including a pixel array (Fig. 1 of Drawings, Specification, page 1, line 10 – page 2, line 6).

Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Saito et al. and Haba et al. (US 6,376,904). As per Claim 3, it differs from Claim 1 rejected above by its limitation of the ESD protection devices impedance being gradually increase from one outermost device to some intermediate device and being decreased from there to another outermost device. Haba et al. disclose the integrated circuit connections layout (Fig. 4A), wherein the outermost connections between the external terminals and the die are the longest and intermediate connections have their lengths gradually reduced toward the center connection. The impedance of the connections is proportional to their length. Saito et al. disclose the ESD protection devices (NT1 – NTn in Fig. 3) having unequal impedances, since the connective trace in area B has larger impedance than the trace in area A. It further discloses compensation of uneven impedances by varying the resistance of the ESD device (shown in Fig. 8, paragraph [0037]). An added correction is roughly proportional to the additional impedance of the connecting trace. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the AAPA solution by

setting the impedances of the ESD protection devices ES1 to ES j being gradually increased and impedances of the ESD protection devices ES j+1 to ES n gradually decrease, (1<j<n), in accordance with the impedance of the connecting lines, because as Saito et al. state (page 1, [0009] – [0011]), such correction will result in uniform distribution of the ESD load to the protective elements.

Regarding Claim 7, it differs from Claim 3 by its limitation of the first and the last ESD protection devices having impedance different from other ESD protection devices. As stated above (see Claim 3 rejection), when conditions of gradually changing impedance are satisfied, the first and the last ESD protection elements will have the impedance lower than other ESD protection devices.

Claims 2, 6, 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Saito et al., and Esch (US 6,118,310). Claims 2, 6 and 11 differ form Claims 1 and 5 rejected above by their limitation of at least one element having a MOS transistor circuit structure and channel widths of the ESD protection devices disposed on outermost sides of the connection area, i.e. ES1 and Esn, are longer than channel widths of the other ESD protection devices. Saito et al. disclose at least one element having a MOS transistor circuit structure (NT 1 – NT n in Fig. 1). As per Claims 2 and 6, Esch discloses setting specific value of the circuit impedance by setting the channel widths of the ESD protection devices (col. 6, lines 10 – 39). Both references have the same problem solving area, namely providing ESD protection for the semiconductor devices and setting the circuit

impedance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the AAPA solution by setting the protection circuit impedance by varying the channel widths of the ESD protection devices according to Esch, because modification of the circuit impedance by varying the channel width will simplify the circuit making the silicide block resistor unnecessary; as well known in the art, the silicide resistors consume a space and often require an additional manufacturing process, and therefore, are not desirable elements in the integrated circuit.

As per Claim 8, Esch discloses setting specific value of the circuit impedance by setting the channel widths of the ESD protection devices (col. 6, lines 10 – 39). Both references have the same problem solving area, namely providing ESD protection for the semiconductor devices and setting the circuit impedance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the AAPA solution by setting the protection circuit impedance by varying the channel widths of the ESD protection devices according to Esch, because modification of the circuit impedance by varying the channel width will simplify the circuit making unnecessary the resistor; as well known in the art, the silicide resistors consume a space and often require an additional manufacturing process, and therefore, are not desirable elements in the integrated circuit.

Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Saito et al., Haba et al. and Esch (US

6,118,310). Claim 4 differs from Claim 2 rejected above by its limitation of the channel width of the ESD protection devices being gradually decreased from one outermost device to some intermediate device and being increased from there to another outermost device. Haba et al. disclose the integrated circuit connections layout (Fig. 4A), wherein the outermost connections between the external terminals and the die are the longest and intermediate connections have their lengths gradually reduced toward the center connection. The impedance of the connections is proportional to their length. Esch discloses setting specific value of the circuit impedance by setting the channel widths of the ESD protection devices (col. 6, lines 10 – 39). Both references have the same problem solving area, namely providing ESD protection for the semiconductor devices and setting the circuit impedance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the AAPA solution by setting the protection circuit impedance by varying the channel widths of the ESD protection devices according to Esch, because modification of the circuit impedance by varying the channel width will simplify the circuit making unnecessary the resistor; as well known in the art, the silicide resistors consume a space and often require an additional manufacturing process, and therefore, are not desirable elements in the integrated circuit and setting particular values of the channel width in **accordance** with the length of connections demonstrated by Haba et al., i.e., the longer connection, the larger the channel width, because this way assures the even distribution of the impedances, and therefore, the IC will be less vulnerable to the ESD event.

Response to Arguments

Applicant's Arguments have been given careful consideration but they have been found non-convincing.

Applicant attacks the Saito et al. reference alleging that the reference does not disclose "ESD devices disposed on outmost sides of a connection area having smaller impedance than other ESD protection devices" (page 7, last paragraph). To support his allegation, Applicant argues that since "Resistance of the resistors in the area A is set higher than resistance of the resistors in the area B by a value corresponding to resistance of parasitic resistance of the signal line included in the area A so that the resistance of the protective elements in the area A and B are the same or almost the same as each other". To support hid allegation, Applicant recites Saito et al: "the protective elements have the same or almost the same resistance as each other" (page 8, 3rd paragraph). This phrase being taken out of context misrepresents the invention. Saito states (see Claim 1), "resistance of the resistors in each of the protective elements is gradually decreased from the pad toward the internal circuit".

Saito et al. use their own terminology different from Applicant's terminology. A meaning of the recited Saito et al. phrase is that the impedance of the transistors and silicide blocks taken together with the trace impedances are the same across the circuit, and as a result, the electrostatic discharge is evenly spread across the protective elements. When the same criteria (i.e. ESD device impedance includes the impedance

of the trace) are applied to the Applicant's invention the same statement is true, i.e. "the protective elements have the same or almost the same resistance as each other".

Examiner defines the protective element as combination of transistor together with the silicide block. In discussions regarding current Application the trace cannot be considered as a part of the protective element, since the protective element is supposed to compensate for uneven trace impedance.

As clearly shown in Fig. 3 and 4 of Saito et al. the protection elements in areas A and B have different impedances since their silicide block resistances are different (r versus r+ rAB in Fig. 3).

Applicant further attacks the Saito et al. reference alleging: "Saito discloses a compensation of uneven resistances, however, the varied resistances according to Saito are the same as each other". Applicant misrepresents the Saito et al. reference, since if it were true the Saito system would not provide the impedance compensation. Saito states (see Claim 1), "a resistance of the resistors in each of the protective elements is gradually decreased from the pad toward the internal circuit".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
3/22/2007

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800